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EXAMINER	
RASHID, DAVID	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/806,172	Applicant(s) OYABU ET AL.	
	Examiner David P. Rashid	Art Unit 2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 17 May 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 3/23/2004.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

All of the examiner's suggestions presented herein below have been assumed for examination purposes, unless otherwise noted.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed for Application No. 2003-081275, filed on 3/24/2003.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description (drawings):

(i) The specification mentions "W", "N" with regard to FIG. 3A, however, "W", "N" are not depicted in the drawing – suggest adding the reference characters to the figure or deleting description from the specification.

(ii) The specification mentions "N", "L" with regard to FIG. 3B, however, "N", "L" are not depicted in the drawing – suggest adding the reference characters to the figure or deleting description from the specification.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description (specification):

(i) FIG. 8 contains reference characters "a", "b", "c", "d", "e", and "f" that are not described in the specification – suggest either adding a description in the specification (without adding new matter) or deleting them from the drawings

(ii) FIG. 9 contains reference characters "a", "b", "c", "d", "e", and "f" that are not described in the specification – suggest either adding a description in the specification (without adding new matter) or deleting them from the drawings

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

6. 37 CFR 1.75(a) reads as follows:

> The specification must conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery.

7. **Claims 1, 2, 12, 13, 14,** and **15** are objected to under 37 CFR 1.75(a) for failing to particularly point out and distinctly claim the subject matter. The phrase "…that is capable of…" is unclear whether or not that particular element is actually performing the function, since it is only capable of performing the function. Something capable of doing something does not necessarily mean that it is actually doing it – suggest deleting the phrase altogether and changing so that function is definite (e.g., claim 1, line 13 cites "…a second memory that is capable of retaining the scaled image data…" that should be changed to "….a second memory that retains the scaled image data…".

Claim Rejections - 35 USC § 101

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The USPTO "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" (Official Gazette notice of 22 November 2005), Annex IV, reads as follows:

> Nonfunctional descriptive material that does not constitute a statutory process, machine, manufacture or composition of matter and should be rejected under 35 U.S.C. Sec. 101. Certain types of descriptive material, such as music, literature, art, photographs and mere arrangements or compilations of facts or data, without any functional interrelationship is not a process, machine, manufacture or composition of matter. USPTO personnel should be prudent in applying the foregoing guidance. Nonfunctional descriptive material may be claimed in combination with other functional descriptive multi-media material on a computer-readable medium to provide

> the necessary functional and structural interrelationship to satisfy the requirements of 35 U.S.C. Sec. 101. The presence of the claimed nonfunctional descriptive material is not necessarily determinative of nonstatutory subject matter. For example, a computer that recognizes a particular grouping of musical notes read from memory and upon recognizing that particular sequence, causes another defined series of notes to be played, defines a functional interrelationship among that data and the computing processes performed when utilizing that data, and as such is statutory because it implements a statutory process.

9. **Claims 14** and **15** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 14 and 15 recite "An image processing program for realizing a processing to a computer..." which does not impart functionality to a computer or computing device, and is thus considered nonfunctional descriptive material. Such nonfunctional descriptive material, in the absence of a functional interrelationship with a computer, does not constitute a statutory process, machine, manufacture or composition of matter and is thus non-statutory per se. Suggest changing to preamble of claims 14 and 15 to the following:

> "A computer-readable medium comprising computer-executable instructions which, when executed by a computer, cause the computer to perform an image processing method comprising:..."

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for

patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. **Claims 1, 3, 12, 13, 14,** and **15** are rejected under 35 U.S.C. 102(b) as being anticipated by Scott et al. (US 5,097,518 A).

Regarding **claim 1**, Scott discloses an image processing apparatus for generating scaled image data that is obtained by scaling the image data according to a specified scaling factor ("Accordingly, an object of the present invention is to provide apparatus and accompanying method(s) for scaling, specifically reducing, an original image for display as part of a composite image by a document workstation in an image management system.", column 4, line 54. In specific "The above and other objects are also accomplished in accordance with the teachings of the present invention by the inventive fractional movement pixel saving reduction scaling technique.", column 5, line 61 described in detail within FIG. 14 through FIG. 16.), the image processing apparatus comprising:

a receiver that receives an input of pixel value information of each pixel which is contained in image data to be processed in raster scan order ("Either prior to start of reduction scaling or while scaling is in process, the pixel values for the source image successively appear on lead 1601 and are successively written into the source image memory under the control of control logic 1640 and counters 1620 and 1630.", column 46, line 27 wherein the receiver is lead 1601 from which the source image memory 1610 receives its pixel value information (image data). The receiver may also be considered the Input-X counter 1620 and Input-Y counter 1630

from which the source image memory 1610 receives its pixel value information (image X,Y address).);

a first memory that stores the pixel value information input in the raster scan order, the first memory having a capacity equal to or less than a main scanning direction width of the image data (It has been assumed for examination purposes that the main scanning direction is the X (horizontal) scanning direction and the subscanning direction is the Y (vertical) scanning direction. "The horizontal, X Address, appears on leads 1625; while the vertical, Y Address, appears on leads 1635. Both of these addresses are collectively applied as a common address to source image memory 1610. This memory stores the a complete bit map of the bi-tonal pixel values that form the source image.", column 46, line 21 wherein the first memory is source image memory 1610. The memory stores the complete bit map of the bi-tonal pixels values of the source image, and thus holds the capacity equal to or less than a main scanning direction width of the image data since the memory capacity is greater.);

a second memory that is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction ("After the scaled image has been fully generated, this image is read from memory 1650 on a serial basis over output lead 1655 under the control of control logic 1640.", column 47, line 9 wherein the second memory is the scaled image memory 1650. As shown in FIG. 16, the input into the scaled image memory 1650 includes that of the X,Y scaled address leads 1677 and 1697, in combination with lead 1647 D_IN which is the data input from the source image. "In response to each high level pixel value appearing on lead 1615, control logic 1640 produces a high level signal on lead 1643 as a write enable signal to scaled

image memory 1650 along with a high level on lead 1647 as the data input to this memory. As a result of these signals, scaled image memory 1650 writes a "one" into its currently addressed location.", column 46, line 34.);

a destination address generator that generates destination address information in the second memory to specify a destination location of the pixel value information stored in the first memory in response to the specified scaling factor ("The integer address outputs produced by counters 1670 and 1690 are applied by leads 1677 and 1697, respectively, to a common address input to scaled image memory 1650.", column 47, line 6 wherein the destination address generator are the counters 1670 and 1690 that generate the X,Y output address unto leads 1677 and 1697 to feed into scaled image memory 1650.); and

a transferring unit that transfers the pixel value information from the first memory to the second memory based on the generated destination address information (FIG. 16 discloses the control logic 1640 that transfers the pixel value information from the first memory to the second memory based on the generated destination address information. "During scaling, each pixel value in the source image that is accessed from memory 1610 is applied over lead 1615 as an input to control logic 1640.", column 46, line 32 from the first memory to the control logic and "In response to each high level pixel value appearing on lead 1615, control logic 1640 produces a high level signal on lead 1643 as a write enable signal to scaled image memory 1650 along with a high level on lead 1647 as the data input to this memory. As a result of these signals, scaled image memory 1650 writes a "one" into its currently addressed location.", column 46, line 34 from the control logic to the second memory. "Prior to the start of reduction scaling, the contents of registers 1670 and 1690 are suitably initialized by control logic 1640 through

multiplexors 1669 and 1689, to one half the values of variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE, respectively.", column 47, line 12 where the control logic 1640 is responsible for the transfer of image from the first memory to the second is based on the generated destination address information.).

Regarding **claim 3**, Scott discloses the image processing apparatus as claimed in claim 1 further comprising:

a dividing unit that divides the image data into pixel blocks of a size defined based on the capacity of the first memory (The lead 1601 as cited in claim 1 may also be considered the dividing unit that also divides the image data into pixel blocks of a size of exactly "one pixel" based on the capacity of the first memory. As long as the image itself is more than one pixel, the lead 1601 feeding data into the source image memory 1610 is naturally divided by the lead 1601 into separate pixels, and hence can be considered the dividing unit.), wherein

the first memory stores the pixel value information contained in the divided pixel block ("Either prior to start of reduction scaling or while scaling is in process, the pixel values for the source image successively appear on lead 1601 and are successively written into the source image memory under the control of control logic 1640 and counters 1620 and 1630.", column 46, line 27 wherein the receiver is lead 1601 from which the source image memory 1610 receives its pixel value information (image data).).

Regarding **claim 12**, Scott discloses an image processing method for generating scaled image data that is obtained by scaling the image data according to a specified scaling factor

("Accordingly, an object of the present invention is to provide apparatus and accompanying method(s) for scaling, specifically reducing, an original image for display as part of a composite image by a document workstation in an image management system.", column 4, line 54. In specific "The above and other objects are also accomplished in accordance with the teachings of the present invention by the inventive fractional movement pixel saving reduction scaling technique.", column 5, line 61 described in detail within FIG. 14 through FIG. 16.), the image processing method comprising:

receiving an input of pixel value information of each pixel which is contained in image data to be processed in raster scan order ("Either prior to start of reduction scaling or while scaling is in process, the pixel values for the source image successively appear on lead 1601 and are successively written into the source image memory under the control of control logic 1640 and counters 1620 and 1630.", column 46, line 27 wherein the receiver is lead 1601 from which the source image memory 1610 receives its pixel value information (image data). The receiver may also be considered the Input-X counter 1620 and Input-Y counter 1630 from which the source image memory 1610 receives its pixel value information (image X,Y address).);

storing the pixel value information input in the raster scan order in a first memory which has a capacity equal to or less than a main scanning direction width of the image data ("The horizontal, X Address, appears on leads 1625; while the vertical, Y Address, appears on leads 1635. Both of these addresses are collectively applied as a common address to source image memory 1610. This memory stores the a complete bit map of the bi-tonal pixel values that form the source image.", column 46, line 21 wherein the first memory is source image memory 1610. The memory stores the complete bit map of the bi-tonal pixels values of the source image, and

thus holds the capacity equal to or less than a main scanning direction width of the image data since the memory capacity is greater.);

generating destination address information in the second memory to specify a destination location of the pixel value information stored in the first memory in response to the specified scaling factor, wherein the second memory is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction ("The integer address outputs produced by counters 1670 and 1690 are applied by leads 1677 and 1697, respectively, to a common address input to scaled image memory 1650.", column 47, line 6 wherein the destination address generator are the counters 1670 and 1690 that generate the X,Y output address unto leads 1677 and 1697 to feed into scaled image memory 1650.

"After the scaled image has been fully generated, this image is read from memory 1650 on a serial basis over output lead 1655 under the control of control logic 1640.", column 47, line 9 wherein the second memory is the scaled image memory 1650. As shown in FIG. 16, the input into the scaled image memory 1650 includes that of the X,Y scaled address leads 1677 and 1697, in combination with lead 1647 D_IN which is the data input from the source image. "In response to each high level pixel value appearing on lead 1615, control logic 1640 produces a high level signal on lead 1643 as a write enable signal to scaled image memory 1650 along with a high level on lead 1647 as the data input to this memory. As a result of these signals, scaled image memory 1650 writes a "one" into its currently addressed location.", column 46, line 34.); and

transferring the pixel value information from the first memory to a second memory based on the generated destination address information (FIG. 16 discloses the control logic 1640 that transfers the pixel value information from the first memory to the second memory based on the generated destination address information. "During scaling, each pixel value in the source image that is accessed from memory 1610 is applied over lead 1615 as an input to control logic 1640.", column 46, line 32 from the first memory to the control logic and "In response to each high level pixel value appearing on lead 1615, control logic 1640 produces a high level signal on lead 1643 as a write enable signal to scaled image memory 1650 along with a high level on lead 1647 as the data input to this memory. As a result of these signals, scaled image memory 1650 writes a "one" into its currently addressed location.", column 46, line 34 from the control logic to the second memory. "Prior to the start of reduction scaling, the contents of registers 1670 and 1690 are suitably initialized by control logic 1640 through multiplexors 1669 and 1689, to one half the values of variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE, respectively.", column 47, line 12 where the control logic 1640 is responsible for the transfer of image from the first memory to the second is based on the generated destination address information.).

Regarding **claim 13**, Scott discloses an image processing method for generating scaled image data that is obtained by scaling the image data according to a specified scaling factor (refer to references/arguments cited in claim 12), the image processing method comprising:

receiving an input of pixel value information of each pixel which is contained in image data to be processed in raster scan order (refer to references/arguments cited in claim 12);

storing the pixel value information input in the raster scan order in a first memory which has a capacity equal to or less than the main scanning direction width of the image data (refer to references/arguments cited in claim 12);

generating a source address information in the first memory that stores the pixel value information to be retained in each address in the second memory, that is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction, based on an address shift amount determined in response to the specified scaling factor ("The address to memory 1650 is formed by adders 1660 and 1680, and Output.sub.-- X and Output.sub.-- Y registers 1670 and 1690.", column 46, line 43 wherein the source address generating unit are the registers 1670 and 1690 and their preceding elements); and

transferring the pixel value information from the first memory to a second memory based on the generated source address information (refer to references/arguments cited in claim 12).

Regarding **claim 14**, Scott discloses an image processing program for realizing a processing to a computer to generate scaled image data that is obtained by scaling the image data according to a specified scaling factor (Refer to references/arguments cited in claim 12. Scott discloses the present invention as an image processing program for realizing a processing to a computer as cited "Disk 225 stores the remainder of the program that will be executed by either central processing unit 220 and the entire program executed by image processor 265.", column 10, line 31.), the image processing method comprising:

receiving an input of pixel value information of each pixel which is contained in image data to be processed in raster scan order; storing the pixel value information input in the raster scan order in a first memory which has a capacity equal to or less than a main scanning direction width of the image data (refer to references/arguments cited in claim 12);

generating destination address information in the second memory to specify a destination location of the pixel value information stored in the first memory in response to the specified scaling factor, wherein the second memory is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction (refer to references/arguments cited in claim 12); and

transferring the pixel value information from the first memory to a second memory based on the generated destination address information (refer to references/arguments cited in claim 12).

Regarding **claim 15**, Scott discloses an image processing program for realizing a processing to a computer to generate scaled image data that is obtained by scaling the image data according to a specified scaling factor (Refer to references/arguments cited in claim 12. Scott discloses the present invention as an image processing program for realizing a processing to a computer as cited "Disk 225 stores the remainder of the program that will be executed by either central processing unit 220 and the entire program executed by image processor 265.", column 10, line 31.), the image processing program comprising:

receiving an input of pixel value information of each pixel which is contained in image data to be processed in raster scan order (refer to references/arguments cited in claim 12);

storing the pixel value information input in the raster scan order in a first memory which has a capacity equal to or less than the main scanning direction width of the image data (refer to references/arguments cited in claim 12);

generating a source address information in the first memory that stores the pixel value information to be retained in each address in the second memory, that is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction, based on an address shift amount determined in response to the specified scaling factor (refer to references/arguments cited in claim 13); and

transferring the pixel value information from the first memory to a second memory based on the generated source address information (refer to references/arguments cited in claim 12).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 2, 4, 5, 6, 7, 8, 9, 10,** and **11** are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination between Scott et al. (US 5,097,518 A) and Shyu et al. (US 5,825,367 A).

Regarding **claim 2**, while Scott discloses an image processing apparatus for generating scaled image data that is obtained by scaling the image data according to a specified scaling factor (refer to references/arguments cited in claim 1), the image processing apparatus comprising:

a receiver that receives an input of pixel value information of each pixel which is contained in image data to be processed in raster scan order (refer to references/arguments cited in claim 1);

a first memory that stores the pixel value information input in the raster scan order, the first memory having a capacity equal to or less than a main scanning direction width of the image data ("After the scaled image has been fully generated, this image is read from memory 1650 on a serial basis over output lead 1655 under the control of control logic 1640.", column 47, line 9 wherein the first memory is the scaled image memory 1650. As shown in FIG. 16, the input into the scaled image memory 1650 includes that of the X,Y scaled address leads 1677 and 1697, in combination with lead 1647 D_IN which is the data input from the source image. "In response to each high level pixel value appearing on lead 1615, control logic 1640 produces a high level signal on lead 1643 as a write enable signal to scaled image memory 1650 along with a high level on lead 1647 as the data input to this memory. As a result of these signals, scaled image memory 1650 writes a "one" into its currently addressed location.", column 46, line 34.);

a source address generating unit that generates a source address information in the first memory that stores the pixel value information to be retained in each address in the second memory based on an address shift amount determined in response to the specified scaling factor

("The address to memory 1650 is formed by adders 1660 and 1680, and Output.sub.-- X and Output.sub.-- Y registers 1670 and 1690.", column 46, line 43 wherein the source address generating unit are the registers 1670 and 1690 and their preceding elements (all of the elements above the output registers in FIG. 16)); and

a transferring unit that transfers the pixel value information from the first memory to the second memory based on the generated source address information ("After the scaled image has been fully generated, this image is read from memory 1650 on a serial basis over output lead 1655 under the control of control logic 1640.", column 47, line 9 wherein the transferring unit is the lead 1655.), Scott does not teach a second memory that is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction.

Shyu discloses an apparatus for real time two-dimensional scaling of a digital image ("...the object of the present invention is to provide an apparatus which is capable of real-time two-dimensional uniform scaling of a digital image.", column 2, line 10) that teaches a second memory that is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction ("The original image is then scaled in a first dimension, and the resulting one-dimensional scaled image is stored in the frame memory. The scaled image is then scaled in a second dimension, and the resulting two-dimensional scaled image is stored in the frame memory before being provided to an output device, such as a computer display or printer.", column 1, line 57.).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the image processing apparatus of Scott to include a second memory of Shya that is capable of retaining the scaled image data as much as the main scanning direction width relative to a main scanning direction and at least a part of the scaled image data relative to a subscanning direction as taught by Shyu to have a memory that completely contains the capacity of the scaled image, and "...to perform variable expansion and shrinkage of the image...", Shyu, column 1, line 53.

Regarding **claim 4**, Scott discloses further comprising:

a dividing unit that divides the image data into pixel blocks of a size defined based on the capacity of the first memory (The lead 1601 as cited in claim 1 may also be considered the dividing unit that also divides the image data into pixel blocks of a size of exactly "one pixel" based on the capacity of the first memory. As long as the image itself is more than one pixel, the lead 1601 feeding data into the source image memory 1610 is naturally divided by the lead 1601 into separate pixels, and hence can be considered the dividing unit.), wherein the first memory stores the pixel value information contained in the divided pixel block ("In response to each high level pixel value appearing on lead 1615, control logic 1640 produces a high level signal on lead 1643 as a write enable signal to scaled image memory 1650 along with a high level on lead 1647 as the data input to this memory.". column 46, line 34.).

Regarding **claim 5**, Scott discloses wherein the source address generating unit generates the source address using an offset value ("The output of these adders is routed via leads 1667 and

1687 and multiplexors 1669 and 1689 to Output.sub.-- X and Output.sub.-- Y registers 1670 and 1690 and clocked therein at successive clock edges during reduction scaling.", column 46, line 51 where the offset value is Output_X and Output_Y from the multiplexors 1669 and 1689.);

the offset value is provided based on a cumulative addition calculation of the address shift amount (As disclosed in FIG. 16, offset values Output_X and Output_Y are based on a cumulative addition calculation of the address shift amounts X-OUTMOVE and Y-OUTMOVE.); and

the source address generating unit includes: a retaining unit that retains at least a decimal place of the offset value at a point after the pixel value information is transferred ("The full contents, i.e. both the integer and non-integer components, of registers 1670 and 1690 are fed back, via leads 1673 and 1693, respectively, to corresponding inputs of adders 1660 and 1680.", column 46, line 61 wherein the retaining unit are the leads 1673 and 1693.).

Regarding **claim 6**, Scott discloses wherein the source address generating unit generates the source addresses using respective offset values relative to the main scanning direction and the subscanning direction (It has been assumed for examination purposes that the main scanning direction is the X (horizontal) scanning direction and the subscanning direction is the Y (vertical) scanning direction. "The output of these adders is routed via leads 1667 and 1687 and multiplexors 1669 and 1689 to Output.sub.-- X and Output.sub.-- Y registers 1670 and 1690 and clocked therein at successive clock edges during reduction scaling.", column 46, line 51 where the offset value is Output_X and Output_Y from the multiplexors 1669 and 1689.);

the respective offset values are provided by performing a cumulative addition calculation of the address shift amounts responsive to the scaling factor in the main scanning direction and that in the subscanning direction (As disclosed in FIG. 16, offset values Output_X and Output_Y are based on a cumulative addition calculation of the address shift amounts X-OUTMOVE and Y-OUTMOVE.); and

the source address generating unit includes: a first retaining unit that retains at least a decimal place of the offset value relative to the main scanning direction at a point after the pixel value information is transferred; and a second retaining unit that retains at least a decimal place of the offset value relative to the subscanning direction ("The full contents, i.e. both the integer and non-integer components, of registers 1670 and 1690 are fed back, via leads 1673 and 1693, respectively, to corresponding inputs of adders 1660 and 1680.", column 46, line 61 wherein the retaining unit are the leads 1673 and 1693.).

Regarding **claim 7**, Scott discloses wherein the source address generating unit further includes:

an initial value retaining unit that retains at least the decimal place of the offset value at the point when the pixel value information has been transferred as much as a capacity of the second memory as an initial value of a next source address calculation, if the second memory cannot retain the pixel value information as much as the subscanning direction width of the scaled image data ("The full contents, i.e. both the integer and non-integer components, of registers 1670 and 1690 are fed back, via leads 1673 and 1693, respectively, to corresponding inputs of adders 1660 and 1680.", column 46, line 61. Regardless of whether the pixel value

information has been transferred as much as a capacity of the second memory as an initial value of a next source address calculation, if the second memory cannot retain the pixel value information as much as the subscanning direction width of the scaled image data, the initial value retaining unit (again, leads 1673 and 1693) retains at least the decimal place of the offset value by transferring the full value every time. Thus, if there ever was a case from which the pixel value information had been transferred as much as a capacity of the second memory as an initial value of a next source address calculation, if the second memory cannot retain the pixel value information as much as the subscanning direction width of the scaled image data, the initial value retaining unit will automatically retain the full offset value which includes at least the decimal place of the offset value.).

Regarding **claim 8**, Scott discloses wherein the address shift amount is a reciprocal of the specified scaling factor (As mentioned in claim 5, X-OUTMOVE and Y-OUTMOVE are the address shift amounts. "As shown, upon entry into process 1400, step 1405 is first performed which assigns the reciprocals of the desired X and Y scale factors, i.e. X.sub.-- SCALEFACTOR and Y.sub.-- SCALEFACTOR, to variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE. X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE store the size of the movement, which is fractional for reduction scaling, in the scaled image that corresponds to a one pixel movement in the input image.", column 43, line 3.); and

the source address generating unit updates the offset value by adding the address shift amount to the current offset value (As disclosed in FIG. 16 the current full value on lead 1673 is fed into adder 1660 with the address shift amount X-OUTMOVE.), and increments the source

address by one if the updated offset value becomes one or more (As mentioned above, the updated offset value is the "full value" being currently updated on lead 1673. Every cycle requires the full value to be added to the reciprocal of the scaling factor (X-OUTMOVE) through adders 1660 and 1680. The combination is then taken through the multiplexer and output register before the full integer value is represented as the address, and the full value is fed back into the adder.

To show that the source address generating unit increments the source address by one if the updated offset value becomes one or more, let us take the scaling factor of 2/3 (reducing the source image 66%) for example. The X-OUTMOVE value is the reciprocal 3/2 (=1.5), and as cited starting from column 47, line 12, divider 1666 initially divides the X-OUTMOVE by 2 before proceeding with the cycles:

Cycle 1: 1 (first source address, full value) + 0.75 (1.5 (X-OUTMOVE) / 2 by divider) = 1.75 (full value) = 1 (integer value)

Cycle 2: 1.75 (full value) + 1.5 (X-OUTMOVE) = 3.25 (full value) = 3 (integer value)

Cycle 3: 3.25 + 1.5 = 4.75 = 4 (integer value)

We then obtain the set {1, 3, 4, 6, 7, 9, 10, 12, 13, …} to obtain the source address locations of the original image to become the scaled image by 2/3. From the set, it can easily be shown a "jump in the address by one" (ex. from 7 to 9, as opposed to "an increment by one" like 9 to 10) occurs when the decimal value of the increasing full value exceeds the value of one (ex. for the jump in source address from 7 to 9, the full value jumps from 7.75 to 9.25, meaning the integer value of the difference in full values is exactly one (9.25 – 7.75 = 1.5 = 1 (integer value)).).

Regarding **claim 9**, Scott discloses wherein the address shift amount is a reciprocal of the specified scaling factor (As mentioned in claim 5, X-OUTMOVE and Y-OUTMOVE are the address shift amounts. "As shown, upon entry into process 1400, step 1405 is first performed which assigns the reciprocals of the desired X and Y scale factors, i.e. X.sub.-- SCALEFACTOR and Y.sub.-- SCALEFACTOR, to variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE. X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE store the size of the movement, which is fractional for reduction scaling, in the scaled image that corresponds to a one pixel movement in the input image.", column 43, line 3.); and

the source address generating unit updates the offset value by adding the address shift amount to the current offset value (As disclosed in FIG. 16 the current full value on lead 1673 is fed into adder 1660 with the address shift amount X-OUTMOVE.), and increments the source address by one if the updated offset value becomes one or more (refer to references/arguments cited in claim 8).

Regarding **claim 10**, Scott discloses wherein the address shift amount is a reciprocal of the specified scaling factor (As mentioned in claim 5, X-OUTMOVE and Y-OUTMOVE are the address shift amounts. "As shown, upon entry into process 1400, step 1405 is first performed which assigns the reciprocals of the desired X and Y scale factors, i.e. X.sub.-- SCALEFACTOR and Y.sub.-- SCALEFACTOR, to variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE. X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE store the size of the movement, which is

fractional for reduction scaling, in the scaled image that corresponds to a one pixel movement in the input image.", column 43, line 3.); and

the source address generating unit updates the offset value by adding the address shift amount to the current offset value (As disclosed in FIG. 16 the current full value on lead 1673 is fed into adder 1660 with the address shift amount X-OUTMOVE.), and increments the source address by one if the updated offset value becomes one or more (refer to references/arguments cited in claim 8).

Regarding **claim 11**, Scott discloses wherein the address shift amount is a reciprocal of the specified scaling factor (As mentioned in claim 5, X-OUTMOVE and Y-OUTMOVE are the address shift amounts. "As shown, upon entry into process 1400, step 1405 is first performed which assigns the reciprocals of the desired X and Y scale factors, i.e. X.sub.-- SCALEFACTOR and Y.sub.-- SCALEFACTOR, to variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE. X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE store the size of the movement, which is fractional for reduction scaling, in the scaled image that corresponds to a one pixel movement in the input image.", column 43, line 3.); and

the source address generating unit

updates the offset value by adding the address shift amount to the current offset value (As disclosed in FIG. 16 the current full value on lead 1673 is fed into adder 1660 with the address shift amount X-OUTMOVE.),

increments the source address by one if the updated offset value becomes one or more (refer to references/arguments cited in claim 8),

refers to a location of the pixel value information stored in the first memory on the image data to be processed ("The integer address outputs produced by counters 1670 and 1690 are applied by leads 1677 and 1697, respectively, to a common address input to scaled image memory 1650.", column 47, line 6), and

sets the offset value to the initial value retained in the initial value retaining unit if the location satisfies a predetermined condition ("Prior to the start of reduction scaling, the contents of registers 1670 and 1690 are suitably initialized by control logic 1640 through multiplexors 1669 and 1689, to one half the values of variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE, respectively. Specifically, an INIT pulse applied to a control (C) input of each multiplexor cause multiplexors 1669 and 1689 to route one half of the value of variables X.sub.-- OUTMOVE and Y.sub.-- OUTMOVE to the inputs of Output.sub.-- X register 1670 and Output.sub.-- Y register 1690.", column 47, line 12. In essence, if the location satisfies the predetermined condition of being null or 0 (prior to the starting of reduction scaling), the offset value is set to the initial value retained in the initial value retaining unit to be one half the values of variables X-OUTMOVE and Y-OUTMOVE.).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David P. Rashid whose telephone number is (571) 270-1578. The examiner can normally be reached on 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Werner can be reached on (571) 272-7401. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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